19-4030; Rev 0; 2/08

# DisplayPort/PCIe Passive Switches



## General Description

The MAX4928A/MAX4928B high-speed passive switches route PCI Express® (PCIe) data and/or DisplayPort™ signals between two possible destinations in desktop or laptop PCs. The MAX4928A is intended to be used with the ATX form factor desktop PCs, while the MAX4928B is expected to be used in the BTX form factor.

The MAX4928A/MAX4928B are hex double-pole/double-throw (6 x DPDT) switches. The MAX4928A/MAX4928B feature a single digital control input (SEL) to switch signal paths and a latch input (LE) that holds the switches in a given state.

The MAX4928A/MAX4928B are fully specified to operate from a single +3.3V (typ) power supply. The MAX4928A/MAX4928B are available in an industry standard 5mm x 11mm, 56-pin TQFN package. Both devices operate over the -40°C to +85°C extended temperature range.

## Applications

Desktop PCs

Notebook PCs

*PCI Express is a registered trademark of PCI-SIG.*

*DisplayPort is a trademark of Video Electronics Standards Association (VESA).*

## Features

- **Single +3.3V Power Supply Voltage**
- **Supports PCIe Gen I, Gen II, and DisplayPort Data Rates > 5Gbps**
- **Excellent Return Loss > 12dB at 2.5GHz**
- **Six Bidirectional Pairs of Switches All Switching in One Device**
- **Low 800µA (max) Supply Current**
- **Small 5mm x 11mm, 56-Pin TQFN Package**
- **Industry Standard Pinouts**

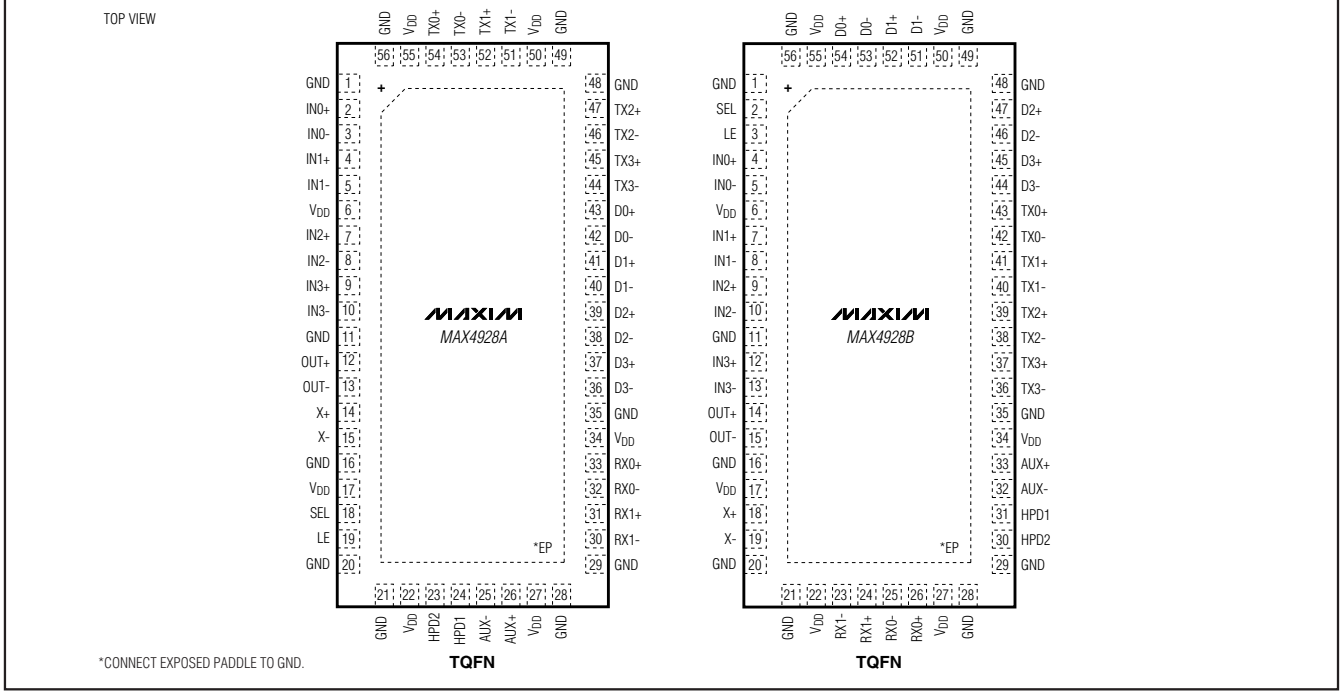
## Ordering Information

| PART | PIN-PACKAGE | PKG CODE |
|---|---|---|
| **MAX4928A**ETN+ | 56 TQFN-EP | T56511-1 |
| **MAX4928B**ETN+ | 56 TQFN-EP | T56511-1 |

***Note:*** *All devices are specified over the -40°C to +85°C temperature range.*
*+Denotes a lead-free package.*
*EP = Exposed paddle.*

***Typical Operating Circuit appears at end of data sheet.***

## Pin Configurations



## ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)
$V_{DD}$ .....-0.3V to +4V
LE, SEL, IN_, X_, OUT_, D_, TX_, HPD_, RX_, AUX_ (Note 1) .....-0.3V to + ($V_{DD}$ + 0.3V)
$|V_{IN\_} - V_{TX\_}|$, $|V_{IN\_} - V_{D\_}|$, $|V_{X\_} - V_{HPD\_}|$, $|V_{X\_} - V_{RX1\_}|$, $|V_{OUT\_} - V_{AUX\_}|$, $|V_{OUT\_} - V_{RX0\_}|$ (Note 1).....0 to +2V
Continuous Current (IN_ to D_/TX_, X_ to HPD_/RX1_, OUT_ to AUX_/RX0_ .....±70mA
Peak Current (IN_ to D_/TX_, X_ to HPD_/RX1_, OUT_ to AUX_/RX0_) (pulsed at 1ms, 10% duty cycle) .....±70mA
Continuous Current (LE, SEL).....±30mA
Peak Current (LE, SEL) (pulsed at 1ms, 10% duty cycle).....±70mA
Continuous Power Dissipation ($T_A$ = +70°C) for Multilayer Board 56-Pin TQFN (derate 41.0mW/°C above +70°C) .....3279mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Package Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) (Note 2) .....24.4°C/W
Package Junction-to-Case Thermal Resistance ($\theta_{JC}$) (Note 2) .....1.5°C/W
Lead Temperature (soldering).....+300°C

**Note 1:** Signals on IN_, X_, OUT_, D_, TX_, HPD_, RX_, or AUX_, LE, SEL exceeding $V_{DD}$ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

**Note 2:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, see www.maxim-ic.com/thermal-tutorial.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = +3.3V ±10%, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $V_{DD}$ = +3.3V, $T_A$ = +25°C, unless otherwise noted.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | |
| Analog Signal Range | IN_, X_, OUT_, D_, TX_, HPD_, RX_, AUX_ | | -0.1 | | ($V_{DD}$ - 1.8) | V |
| Voltage Between IN and D/TX, X and HPD/RX1, and OUT and AUX/RX0 | $\|V_{IN\_} - V_{TX\_}\|$, $\|V_{IN\_} - V_{D\_}\|$, $\|V_{X\_} - V_{HPD\_}\|$, $\|V_{X\_} - V_{RX1\_}\|$, $\|V_{OUT\_} - V_{AUX\_}\|$, $\|V_{OUT\_} - V_{RX0\_}\|$ | | 0 | | 1.8 | V |
| On-Resistance | $R_{ON}$ | $I_{IN\_}$ = $I_{X\_}$ = $I_{OUT\_}$ = 15mA, $V_{D\_}$, $V_{TX\_}$, $V_{HPD\_}$, $V_{AUX\_}$, or $V_{RX\_}$ = 0V, +1.2V | | 8 | | Ω |
| On-Resistance Match Between Pairs of Same Channel | $\Delta R_{ON}$ | $V_{DD}$ = +3.0V, $I_{IN\_}$ = $I_{X\_}$ = $I_{OUT\_}$ = 15mA, $V_{D\_}$, $V_{TX\_}$, $V_{HPD\_}$, $V_{AUX\_}$, or $V_{RX\_}$ = 0V (Notes 4, 5) | | 0.1 | 1 | Ω |
| On-Resistance Match Between Channels | $\Delta R_{ON}$ | $V_{DD}$ = +3.0V, $I_{IN\_}$ = $I_{X\_}$ = $I_{OUT\_}$ = 15mA, $V_{D\_}$, $V_{TX\_}$, $V_{HPD\_}$, $V_{AUX\_}$, or $V_{RX\_}$ = 0V (Notes 4, 5) | | 1.5 | 4 | |
| On-Resistance Flatness | $R_{FLAT(ON)}$ | $V_{DD}$ = +3.0V, $I_{IN\_}$ = $I_{X\_}$ = $I_{OUT\_}$ = 15mA, $V_{D\_}$, $V_{TX\_}$, $V_{HPD\_}$, $V_{AUX\_}$, or $V_{RX\_}$ = 0V, +1.2V (Notes 5, 6) | | 3 | 1.5 | Ω |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = +3.3V ±10%, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $V_{DD}$ = +3.3V, $T_A$ = +25°C, unless otherwise noted.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| D_ or TX_/ HPD_ or RX1_/ AUX_ or RX0_ Off-Leakage Current | $I_{D\_(OFF)}$ $I_{TX\_(OFF)}$ $I_{HPD\_(OFF)}$ $I_{RX1\_(OFF)}$ $I_{AUX\_(OFF)}$ $I_{RX0\_(OFF)}$ | $V_{DD}$ = +3.6V , $V_{IN\_}$ = $V_{X\_}$ = $V_{OUT\_}$ = 0V, +1.2V; $V_{D\_}$ or $V_{TX\_}$, $V_{HPD\_}$ or $V_{RX1\_}$, $V_{AUX\_}$ or $V_{RX0\_}$ = +1.2V, 0V | -1 | | +1 | µA |
| IN_/X_/OUT_ On-Leakage Current | $I_{IN\_(ON)}$ $I_{X\_(ON)}$ $I_{OUT\_(ON)}$ | $V_{DD}$ = +3.6V , $V_{IN\_}$ = $V_{X\_}$ = $V_{OUT\_}$ = 0V, +1.2V; $V_{D\_}$ or $V_{TX\_}$ = $V_{IN\_}$ or unconnected, $V_{HPD\_}$ or $V_{RX1\_}$ = $V_{X\_}$ or unconnected, $V_{AUX\_}$ or $V_{RX0\_}$ = $V_{OUT\_}$ or unconnected | -1 | | +1 | |
| **DIGITAL SIGNALS** | | | | | | |
| SEL to Switch Turn-On Time | $t_{ON\_SEL}$ | $V_{D\_}$ or $V_{TX\_}$ = +1.0V, $R_L$ = 50Ω, $V_{HPD\_}$ or $V_{RX1\_}$ = +1.0V, $R_L$ = 50Ω, $V_{AUX\_}$ or $V_{RX0\_}$ = +1.0V, $R_L$ = 50Ω, LE = $V_{DD}$, $C_L$ = 100pf (Figure 1) | | 55 | 120 | ns |
| SEL to Switch Turn-Off Time | $t_{OFF\_SEL}$ | $V_{D\_}$ or $V_{TX\_}$ = +1.0V, $R_L$ = 50Ω, $V_{HPD\_}$ or $V_{RX1\_}$ = +1.0V, $R_L$ = 50Ω, $V_{AUX\_}$ or $V_{RX0\_}$ = +1.0V, $R_L$ = 50Ω, LE = $V_{DD}$, $C_L$ = 100pf (Figure 1) | | 8 | 50 | ns |
| LE Setup Time SEL to LE | $t_{SU}$ | $V_{D\_}$ or $V_{TX\_}$ = +1.0V, $R_L$ = 50Ω, $V_{HPD\_}$ or $V_{RX1\_}$ = +1.0V, $R_L$ = 50Ω, $V_{AUX\_}$ or $V_{RX0\_}$ = +1.0V, $R_L$ = 50Ω (Figure 1) | | 2 | | ns |
| LE Hold Time SEL to LE | $t_{HOLD}$ | $V_{D\_}$ or $V_{TX\_}$ = +1.0V, $R_L$ = 50Ω, $V_{HPD\_}$ or $V_{RX1\_}$ = +1.0V, $R_L$ = 50Ω, $V_{AUX\_}$ or $V_{RX0\_}$ = +1.0V, $R_L$ = 50Ω, (Figure 1) | | 2 | | ns |
| LE Minimum Pulse-Width Low | $t_W$ | $V_{D\_}$ or $V_{TX\_}$ = +1.0V, $R_L$ = 50Ω, $V_{HPD\_}$ or $V_{RX1\_}$ = +1.0V, $R_L$ = 50Ω, $V_{AUX\_}$ or $V_{RX0\_}$ = +1.0V, $R_L$ = 50Ω (Figure 1) | 40 | | | ns |
| Differential Insertion Loss (Figure 2) | $S_{DD21}$ | f = 2.5GHz | | -1.5 | | dB |
| | | f = 5.0GHz | | -3.3 | | |
| | | f = 7.5GHz | | -4.9 | | |
| Differential Crosstalk (Figure 2) | $S_{DDCTK}$ | f = 2.5GHz | | -40 | | dB |
| | | f = 5.0GHz | | -23 | | |
| | | f = 7.5GHz | | -28 | | |
| Differential Off-Isolation | $S_{DD21\_OFF}$ | f = 3.0GHz | | -22 | | dB |
| Differential Return Loss (Figure 2) | $S_{DD11}$ | f = 2.8GHz | | -21 | | dB |
| | | f = 5.0GHz | | -8 | | |
| | | f = 7.5GHz | | -7 | | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = +3.3V ±10%, $T_A$ =$T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $V_{DD}$ = +3.3V, $T_A$ = +25°C, unless otherwise noted.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Signal Data Rate | BR | $R_S$ = $R_L$ = 100Ω balanced | | 10 | | Gbps |
| Differential -3dB Bandwidth | DBW | $R_S$ = $R_L$ = 100Ω balanced | | 5 | | GHz |
| **LOGIC INPUT (LE, SEL)** | | | | | | |
| Input Logic-High | $V_{IH}$ | | 1.4 | | | V |
| Input Logic-Low | $V_{IL}$ | | | | 0.5 | V |
| Input Logic Hysteresis | $V_{HYST}$ | | | 100 | | mV |
| Input Leakage Current | $I_{IN}$ | $V_{IN}$ = 0 or $V_{DD}$ | -1 | | +1 | µA |
| **POWER SUPPLY** | | | | | | |
| Power Supply Range | $V_{DD}$ | | 3.0 | | 3.6 | V |
| $V_{DD}$ Supply Current | $I_{DD}$ | $V_{IN}$ = 0 or $V_{DD}$ | | | 850 | µA |

**Note 3:** All units are 100% production tested at $T_A$ = +85°C. Limits over the operating temperature range are guaranteed by design and characterization and are not production tested.

**Note 4:** $\Delta R_{ON} = R_{ON\,(MAX)} - R_{ON\,(MIN)}$.

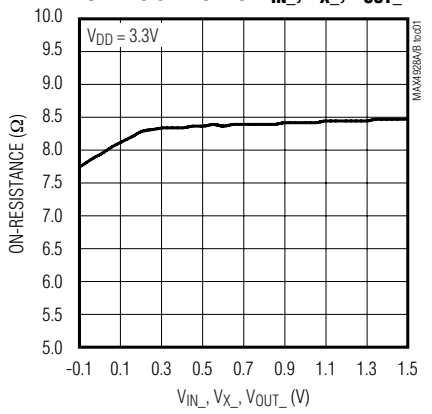
**Note 5:** Guaranteed by design. Not production tested.

**Note 6:** Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

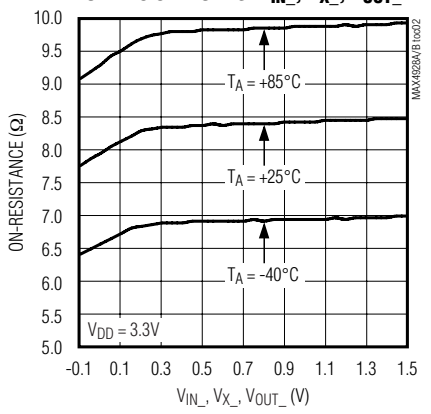
## Typical Operating Characteristics

($T_A$ = +25°C, unless otherwise noted.)

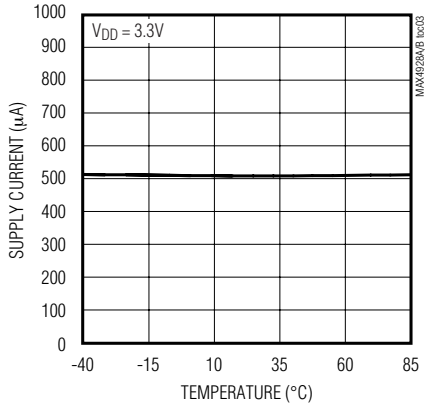
**ON-RESISTANCE vs. $V_{IN\_}$, $V_{X\_}$, $V_{OUT\_}$**



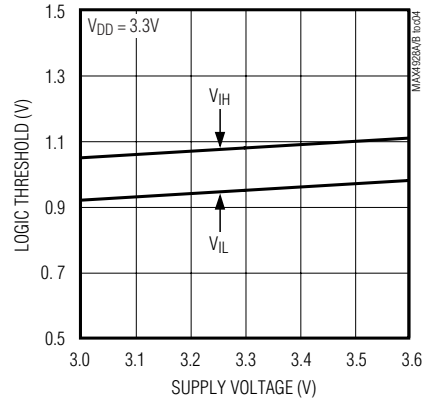

**ON-RESISTANCE vs. $V_{IN\_}$, $V_{X\_}$, $V_{OUT\_}$**



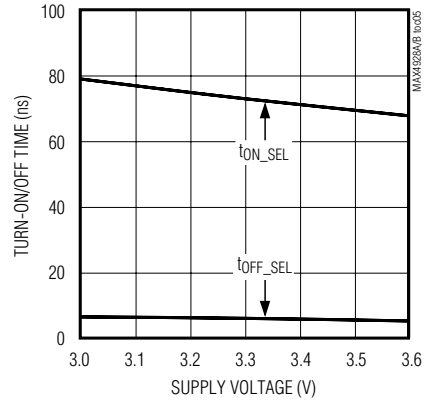

**SUPPLY CURRENT vs. TEMPERATURE**



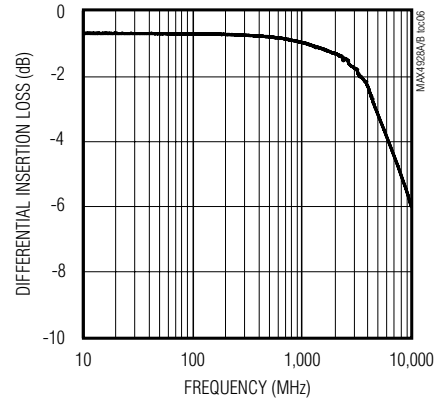

**LOGIC THRESHOLD vs. SUPPLY VOLTAGE**



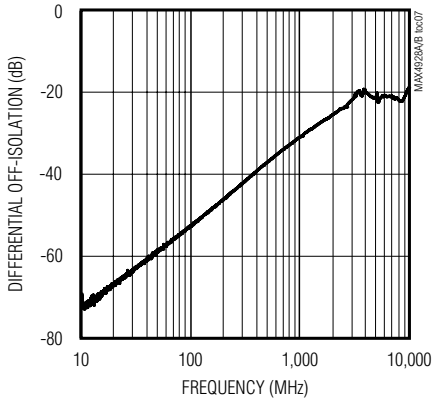

**TURN-ON/OFF TIME vs. SUPPLY VOLTAGE**



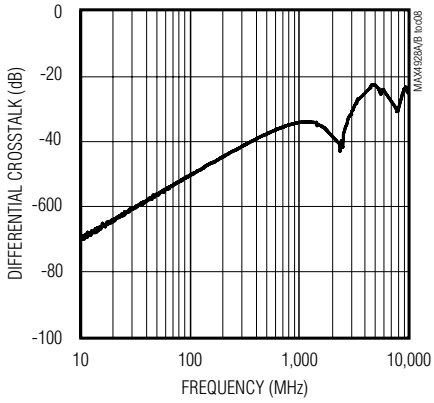

**DIFFERENTIAL INSERTION LOSS**



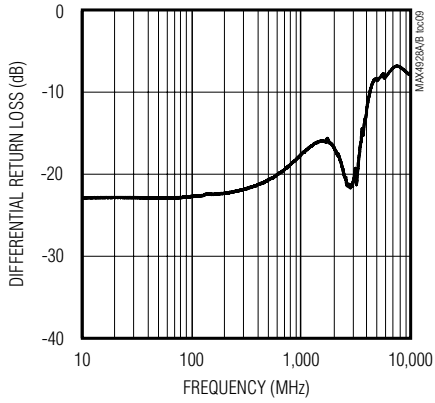

**DIFFERENTIAL OFF-ISOLATION**




**DIFFERENTIAL CROSSTALK**




**DIFFERENTIAL RETURN LOSS**



# DisplayPort/PCIe Passive Switches

## Test Circuits/Timing Diagrams

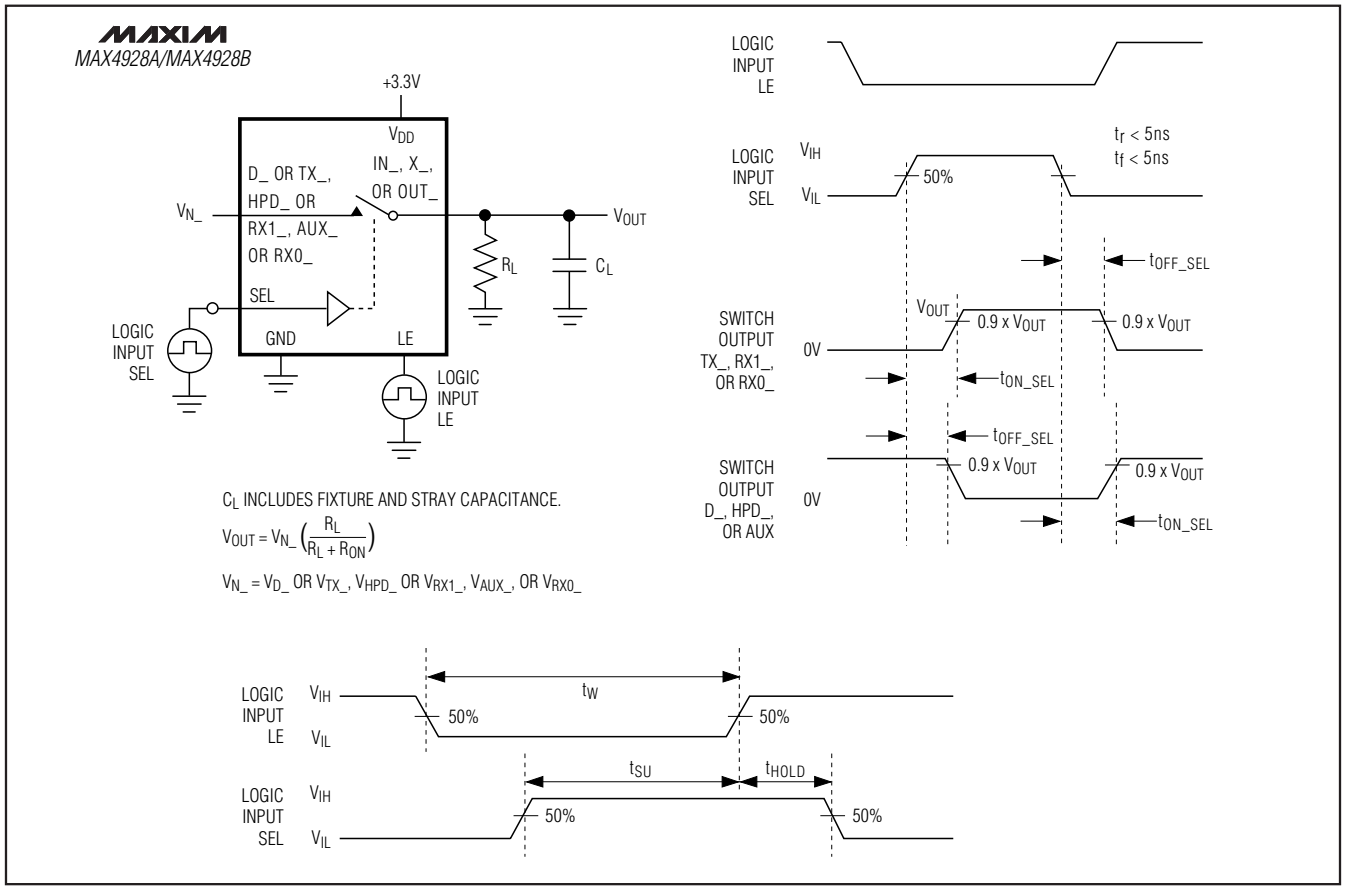
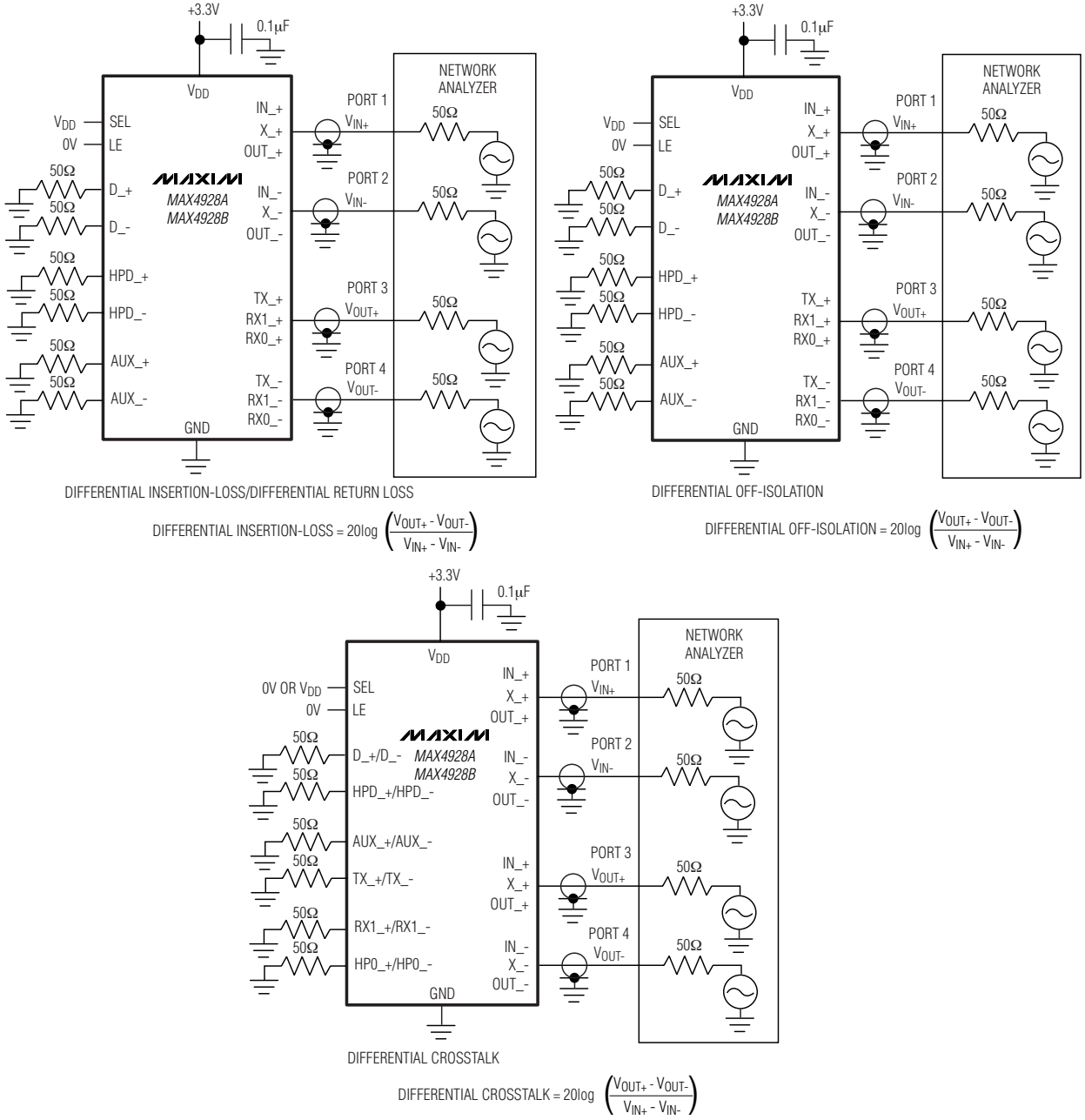



*Figure 1. Switching Time*

## Test Circuits/Timing Diagrams (continued)




MEASUREMENTS ARE STANDARDIZED AGAINST SHORTS AT IC TERMINALS.
DIFFERENTIAL OFF-ISOLATION IS MEASURED BETWEEN IN_ AND "OFF" D_ OR TX_, X_ AND "OFF" HPD_ OR RX1_, OUT_ AND "OFF" AUX_ OR RX0_ TERMINAL ON EACH SWITCH.
DIFFERENTIAL ON-LOSS IS MEASURED BETWEEN IN_ AND "ON" D_ OR TX_, X_ AND "ON" HPD_ OR RX1_, OUT_ AND "ON" AUX_ OR RX0_ TERMINAL ON EACH SWITCH.
DIFFERENTIAL CROSSTALK IS MEASURED BETWEEN ANY TWO PAIRS.

*Figure 2. Differential On-Loss, Differential Off-Isolation, and Differential Crosstalk*

## Pin Description

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX4928A | MAX4928B | | |
| 1, 11, 16, 20, 21, 28, 29, 35, 48, 49, 56 | 1, 11, 16, 20, 21, 28, 29, 35, 48, 49, 56 | GND | Ground |
| 2 | 4 | IN0+ | Analog Switch 1—Common Positive Terminal |
| 3 | 5 | IN0- | Analog Switch 1—Common Negative Terminal |
| 4 | 7 | IN1+ | Analog Switch 2—Common Positive Terminal |
| 5 | 8 | IN1- | Analog Switch 2—Common Negative Terminal |
| 6, 17, 22, 27, 34, 50, 55 | 6, 17, 22, 27, 34, 50, 55 | $V_{DD}$ | Positive Supply Voltage Input. Connect $V_{DD}$ to a +3.0V to +3.6V supply voltage. Bypass $V_{DD}$ to GND with a 0.1µF ceramic capacitor placed as close as possible to the device. See the *Board Layout* section. |
| 7 | 9 | IN2+ | Analog Switch 3—Common Positive Terminal |
| 8 | 10 | IN2- | Analog Switch 3—Common Negative Terminal |
| 9 | 12 | IN3+ | Analog Switch 4—Common Positive Terminal |
| 10 | 13 | IN3- | Analog Switch 4—Common Negative Terminal |
| 12 | 14 | OUT+ | Analog Switch 5—Common Positive Terminal |
| 13 | 15 | OUT- | Analog Switch 5—Common Negative Terminal |
| 14 | 18 | X+ | Analog Switch 6—Common Positive Terminal |
| 15 | 19 | X- | Analog Switch 6—Common Negative Terminal |
| 18 | 2 | SEL | Control Signal Input |
| 19 | 3 | LE | Latch Enable Input |
| 23 | 30 | HPD2 | Analog Switch 6—Normally Open Negative Terminal |
| 24 | 31 | HPD1 | Analog Switch 6—Normally Open Positive Terminal |
| 25 | 32 | AUX- | Analog Switch 5—Normally Open Negative Terminal |
| 26 | 33 | AUX+ | Analog Switch 5—Normally Open Positive Terminal |
| 30 | 23 | RX1- | Analog Switch 6—Normally Closed Negative Terminal |
| 31 | 24 | RX1+ | Analog Switch 6—Normally Closed Positive Terminal |
| 32 | 25 | RX0- | Analog Switch 5—Normally Closed Negative Terminal |
| 33 | 26 | RX0+ | Analog Switch 5—Normally Closed Positive Terminal |
| 36 | 44 | D3- | Analog Switch 4—Normally Open Negative Terminal |
| 37 | 45 | D3+ | Analog Switch 4—Normally Open Positive Terminal |
| 38 | 46 | D2- | Analog Switch 3—Normally Open Negative Terminal |
| 39 | 47 | D2+ | Analog Switch 3—Normally Open Positive Terminal |
| 40 | 51 | D1- | Analog Switch 2—Normally Open Negative Terminal |
| 41 | 52 | D1+ | Analog Switch 2—Normally Open Positive Terminal |
| 42 | 53 | D0- | Analog Switch 1—Normally Open Negative Terminal |
| 43 | 54 | D0+ | Analog Switch 1—Normally Open Positive Terminal |
| 44 | 36 | TX3- | Analog Switch 4—Normally Closed Negative Terminal |
| 45 | 37 | TX3+ | Analog Switch 4—Normally Closed Positive Terminal |
| 46 | 38 | TX2- | Analog Switch 3—Normally Closed Negative Terminal |

## Pin Description (continued)

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX4928A | MAX4928B | | |
| 47 | 39 | TX2+ | Analog Switch 3—Normally Closed Positive Terminal |
| 51 | 40 | TX1- | Analog Switch 2—Normally Closed Negative Terminal |
| 52 | 41 | TX1+ | Analog Switch 2—Normally Closed Positive Terminal |
| 53 | 42 | TX0- | Analog Switch 1—Normally Closed Negative Terminal |
| 54 | 43 | TX0+ | Analog Switch 1—Normally Closed Positive Terminal |
| — | — | EP | Exposed Pad. Connect EP to GND. Exposed pad internally connected to GND. |

## Detailed Description

The MAX4928A/MAX4928B high-speed passive switches route PCI Express (PCIe) data and/or DisplayPort signals between two possible destinations. The MAX4928A/MAX4928B are ideal for routing signals between a graphics memory controller hub (GMCH) and either a DisplayPort or PCIe connector.

The MAX4928A/MAX4928B feature a single digital control input (SEL) to switch signal paths and a latch input (LE) that holds the switches in a given state.

### Digital Control Input (SEL)

The MAX4928A/MAX4928B provide a single digital control input (SEL) to select the signal path between the IN_ and D_/TX_, X_ and HPD_/RX1_, and OUT_ and AUX_/RX0_ channels. The truth tables for the MAX4928A/MAX4928B are depicted in the *Functional Diagrams/Truth Table*. Drive SEL rail-to-rail to minimize power consumption.

### Latch Control Input (LE)

The MAX4928A/MAX4928B provide a single digital control input (LE) to latch the signal paths between the IN_ and D_/TX_, X_ and HPD_/RX1_, and OUT_ and AUX_/RX0_ channels. When LE is driven high, the switches are held in their previous state, regardless of the input signal to SEL. Drive LE rail-to-rail to minimize power consumption.

### Analog Signal Levels

The MAX4928A/MAX4928B accept standard PCIe signals to a maximum of ($V_{DD}$ - 1.8V). Signals on the IN_+ channels are routed to either the D_+ or TX_+ channels, signals on the X+ channel are routed to either HPD1 or RX1+ channels, and signals on the OUT+ channel are routed to either AUX+ or RX0+ channels. Signals on the IN_- channels are routed to either the D_- or TX_- channels, signals on the X- channel are routed to either HPD2 or RX1- channels, and signals on the OUT- channel are routed to either AUX- or RX0- channels. The MAX4928A/MAX4928B are bidirectional switches, allowing IN_, X_, OUT_, D_, TX_, HPD_, RX_, and AUX_ to be used as either inputs or outputs.

## Applications Information

### DisplayPort/PCIe Switching

The MAX4928A/MAX4928B primary applications are aimed to switch between a GMCH and either a DisplayPort or PCIe connector. The MAX4928A/MAX4928B contain n-channel switches to permit differential signals to be selected between a PCIe Gen II socket or to a DisplayPort connector. Each device handles up to six pairs of signals. The DisplayPort signal is an AC-coupled 8b/10b encoded differential signal ranging up to 2.7 Gbps. The PCIe Gen I and Gen II signals are AC-coupled, 8b/10b encoded differential signals ranging up to 5.0Gbps.

### Board Layout

High-speed switches require proper layout and design procedures for optimum performance. Keep design-controlled impedance PCB traces as short as possible or follow impedance layouts per the PCIe specification. Ensure that power-supply bypass capacitors are placed as close as possible to the device. Multiple bypass capacitors are recommended. Connect all grounds and the exposed pad to large ground planes.

## Chip Information

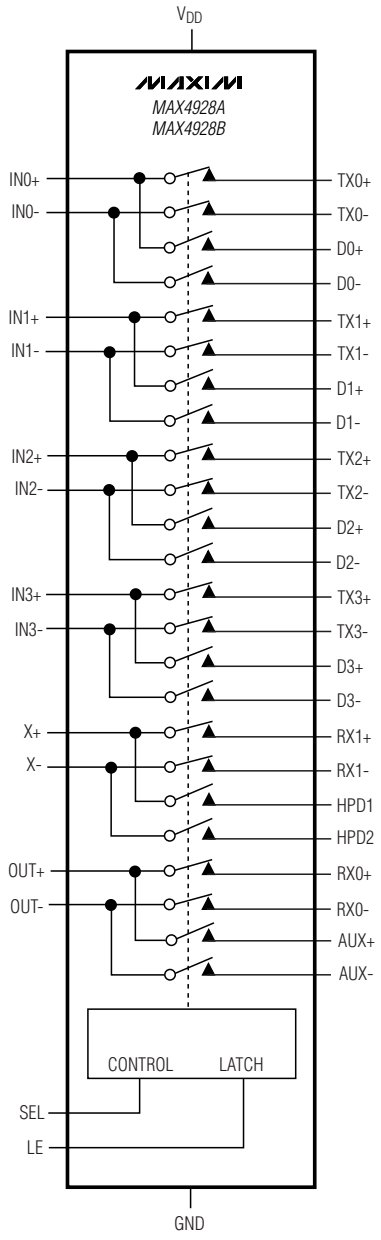
PROCESS: CMOS

# DisplayPort/PCIe Passive Switches

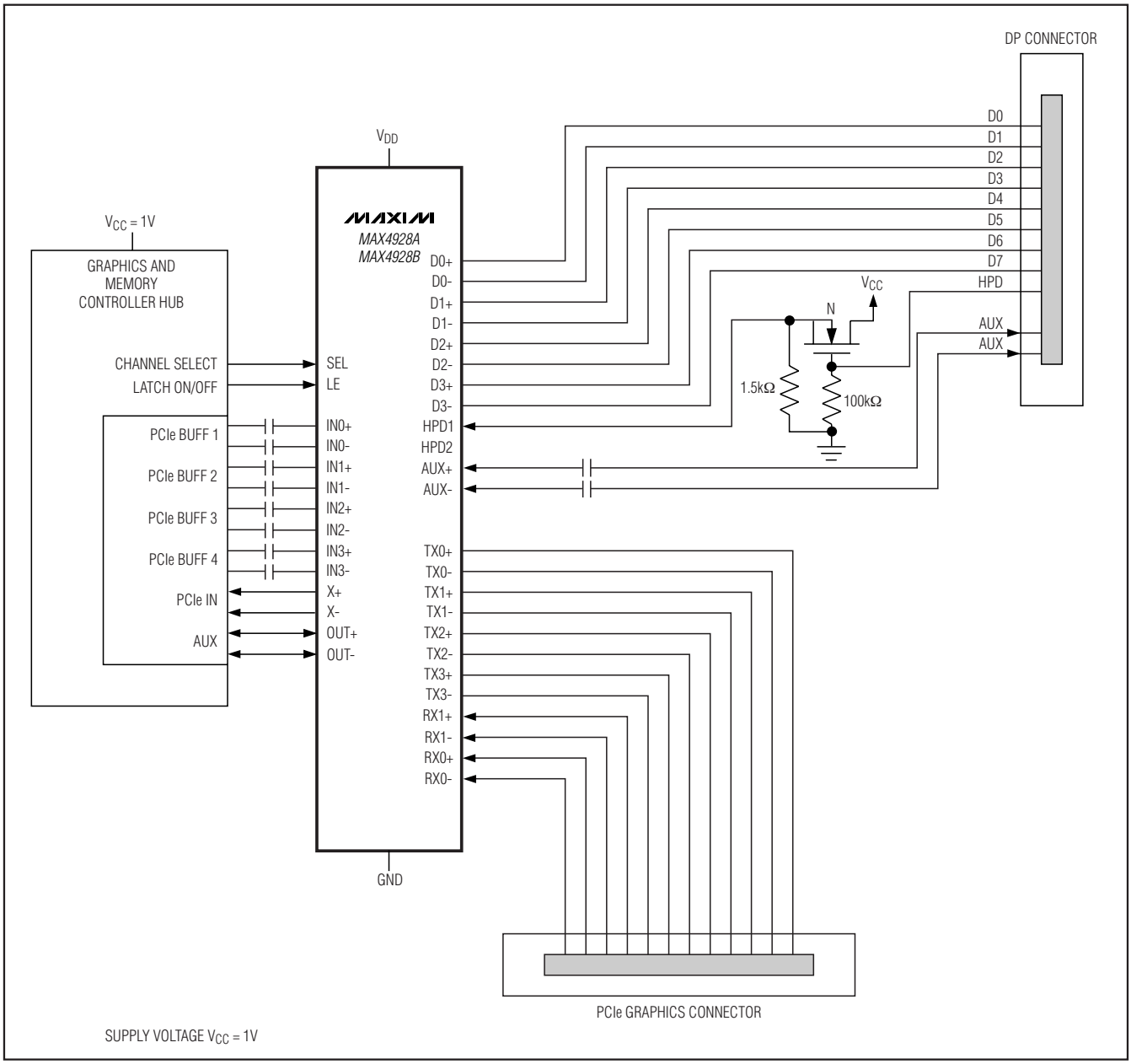
## Functional Diagram/Truth Table

| LE | SEL | IN_ TO TX_, X_ TO RX1_, OUT_ TO RX0_ | IN_ TO DO_, X_ TO HPD_, OUT_ TO AUX_ |
|---|---|---|---|
| 1 | X | NO CHANGE | NO CHANGE |
| 0 | 0 | ON | OFF |
| 0 | 1 | OFF | ON |

X = DON'T CARE.



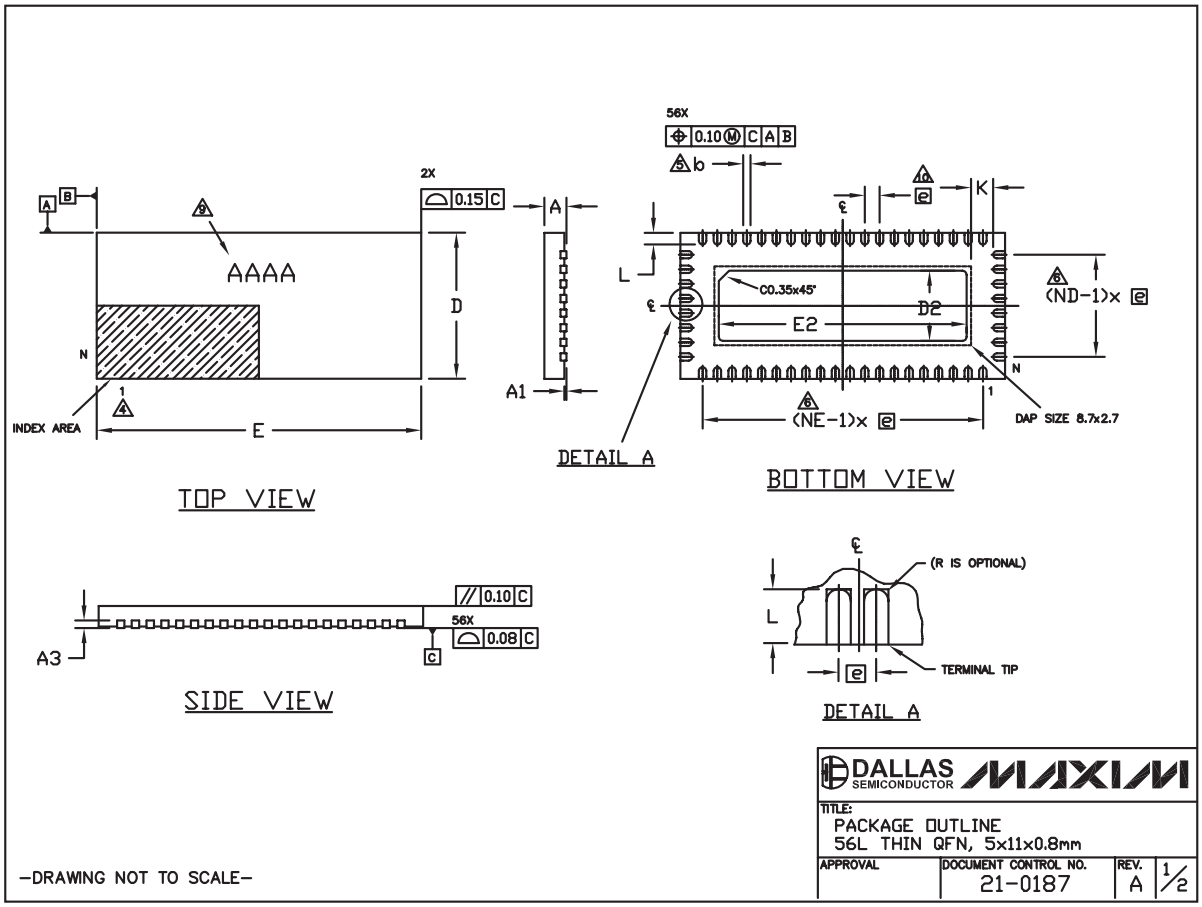
## Typical Operating Circuit



# DisplayPort/PCIe Passive Switches

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

| COMMON DIMENSIONS | | | | |
|---|---|---|---|---|
| REF. | MIN. | NOM. | MAX. | NOTE |
| A | 0.70 | 0.75 | 0.80 | |
| A1 | 0 | – | 0.05 | |
| A3 | | 0.20 REF. | | |
| b | 0.20 | 0.25 | 0.30 | |
| D | 4.90 | 5.00 | 5.10 | |
| E | 10.90 | 11.00 | 11.10 | |
| e | | 0.50 BSC. | | |
| k | 0.25 | – | – | |
| L | 0.30 | 0.40 | 0.50 | |
| N | | 56 | | |
| ND | | 8 | | |
| NE | | 20 | | |

| | EXPOSED PAD VARIATIONS | | | | | |
|---|---|---|---|---|---|---|
| | D2 | | | E2 | | |
| PKG. CODE | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| T56511-1 | 2.30 | 2.40 | 2.50 | 8.30 | 8.40 | 8.50 |

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
8. WARPAGE SHALL NOT EXCEED 0.10mm.
9. MARKING IS FOR PACKAGE ORIENTATION PURPOSE ONLY.
10. LEAD CENTERLINES TO BE AT DEFINED BY DIMESION e ±0.05.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE 56L THIN QFN, 5x11x0.8mm

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0187 | A | 2/2 |